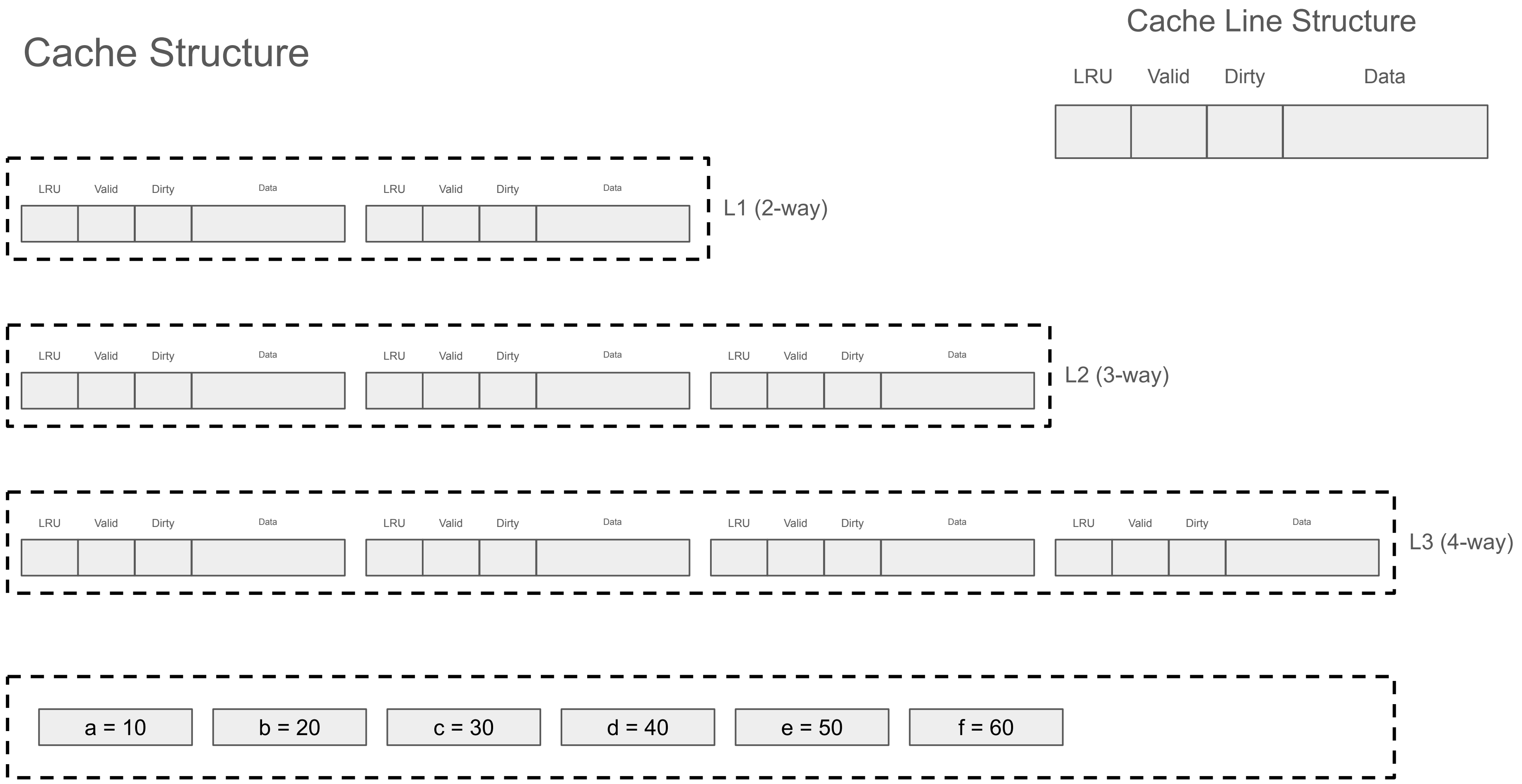
Cache Access Path

Spring 2025 ICS Team

Cache Structure



Initialize

Tick 0

L1 (2-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
0	0	0		0	0	0	

L2 (3-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
0	0	0		0	0	0		0	0	0	

L3 (4-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
0	0	0		0	0	0		0	0	0		0	0	0	

Memory

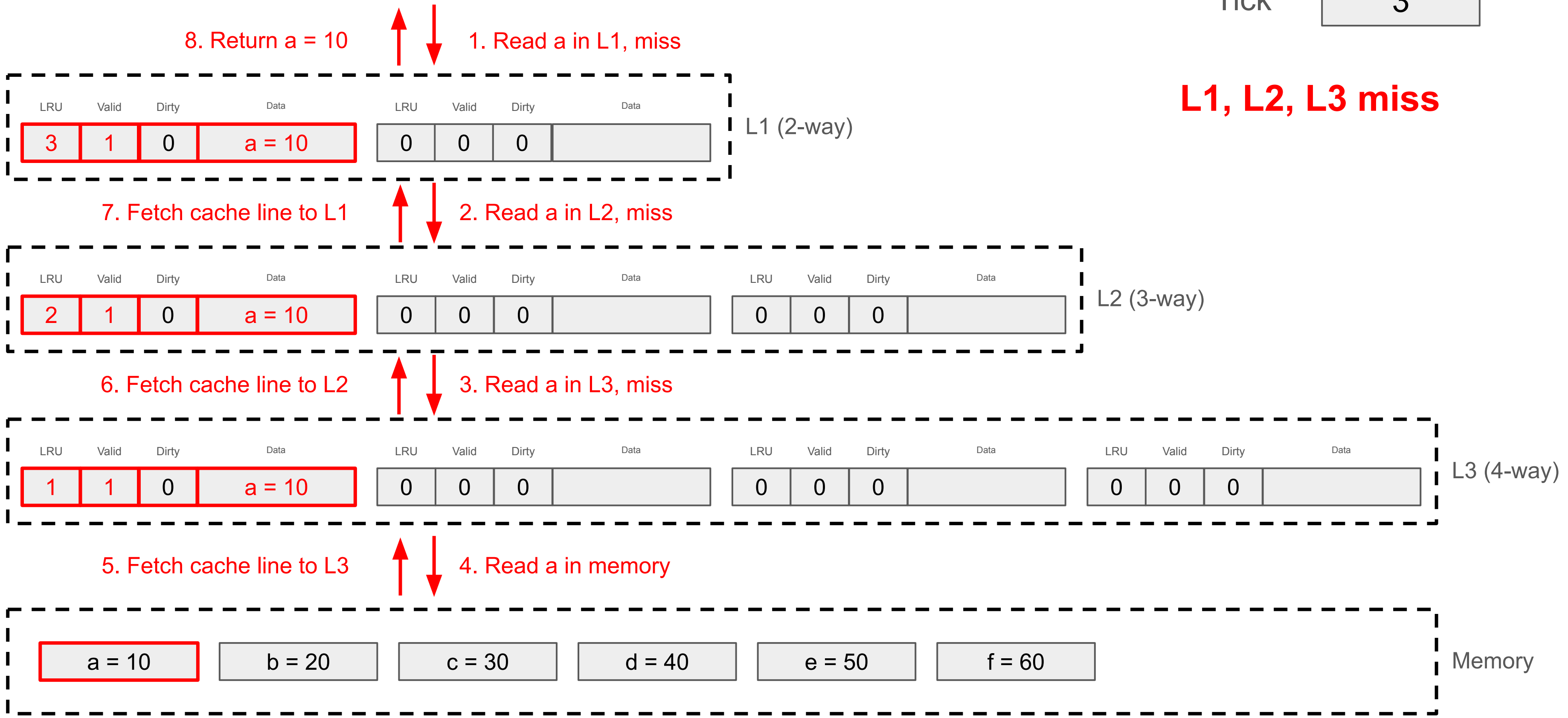
a = 10	b = 20	c = 30	d = 40	e = 50	f = 60

Cache line affected

Read a

Tick 3

L1, L2, L3 miss

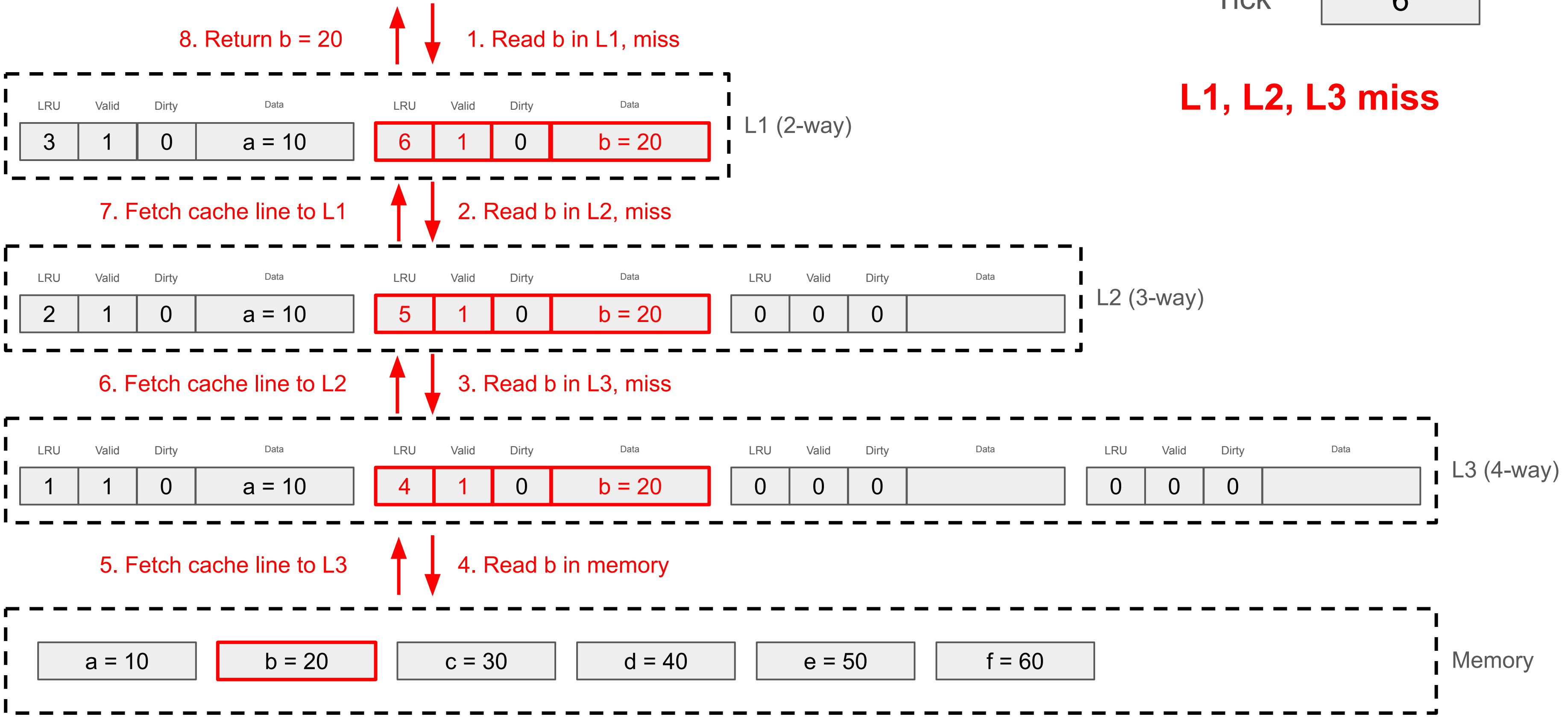


Read b

Cache line affected

Tick 6

L1, L2, L3 miss



L1 (2-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
3	1	0	a = 10	6	1	0	b = 20

L2 (3-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
2	1	0	a = 10	5	1	0	b = 20	0	0	0	

L3 (4-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
1	1	0	a = 10	4	1	0	b = 20	0	0	0		0	0	0	

Memory

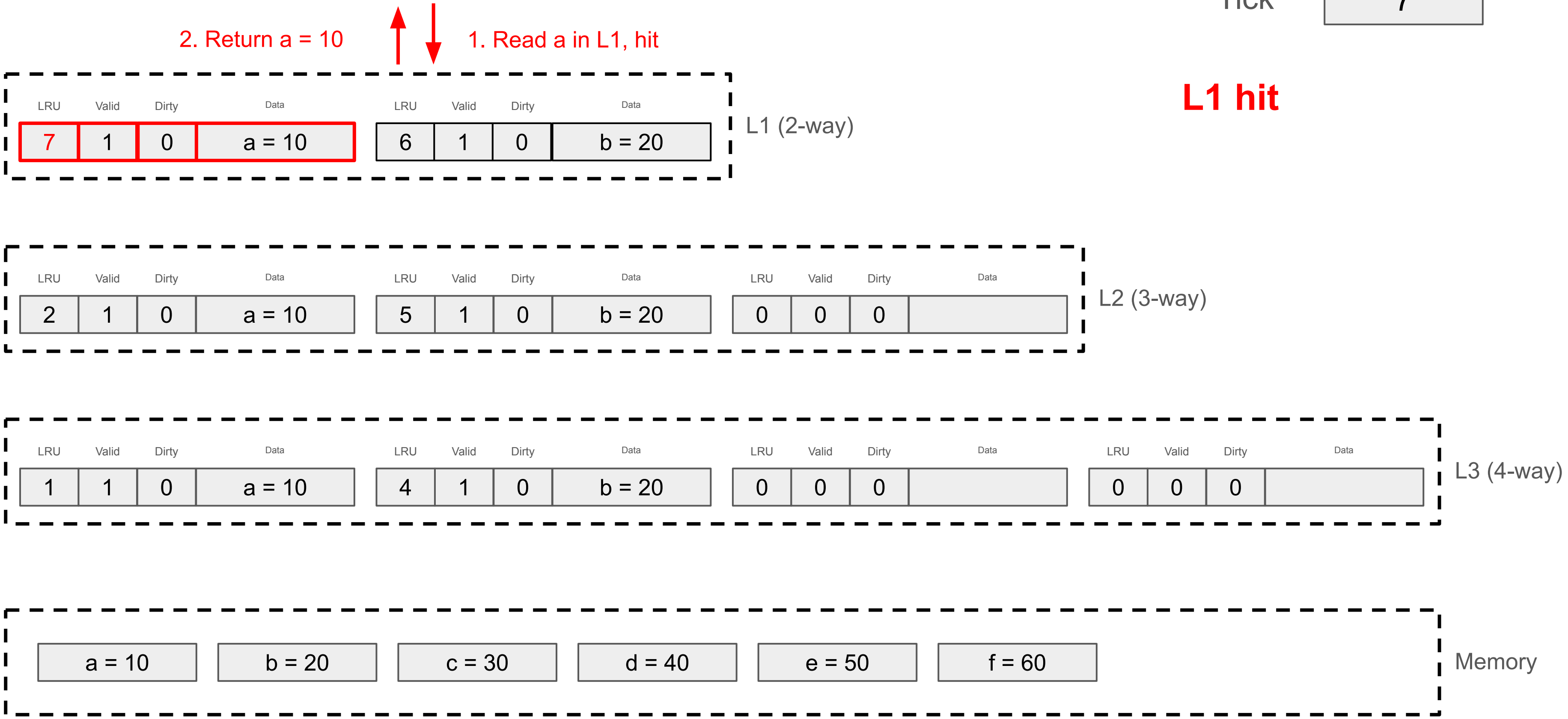
a = 10	b = 20	c = 30	d = 40	e = 50	f = 60

Read a

Cache line affected

Tick 7

L1 hit



L1 (2-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
7	1	0	a = 10	6	1	0	b = 20

L2 (3-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
2	1	0	a = 10	5	1	0	b = 20	0	0	0	

L3 (4-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
1	1	0	a = 10	4	1	0	b = 20	0	0	0		0	0	0	

Memory

a = 10	b = 20	c = 30	d = 40	e = 50	f = 60

Cache line affected

Write b

Tick 8

L1 hit

2. Write b = 21 and return

1. Write b = 21 in L1, hit

L1 (2-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
7	1	0	a = 10	8	1	1	b = 21

L2 (3-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
2	1	0	a = 10	5	1	0	b = 20	0	0	0	

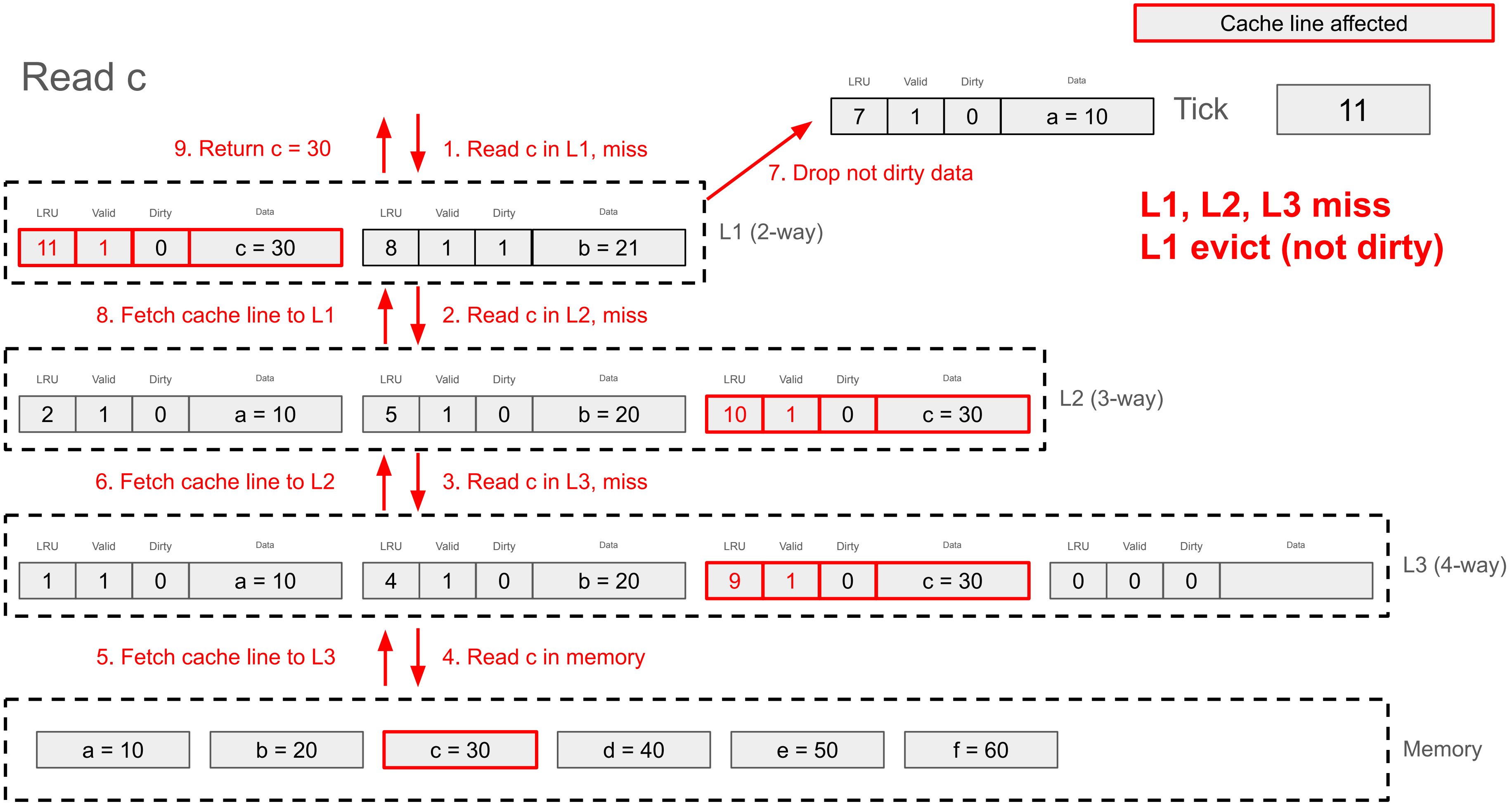
L3 (4-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
1	1	0	a = 10	4	1	0	b = 20	0	0	0		0	0	0	

Memory

a = 10	b = 20	c = 30	d = 40	e = 50	f = 60

Read c



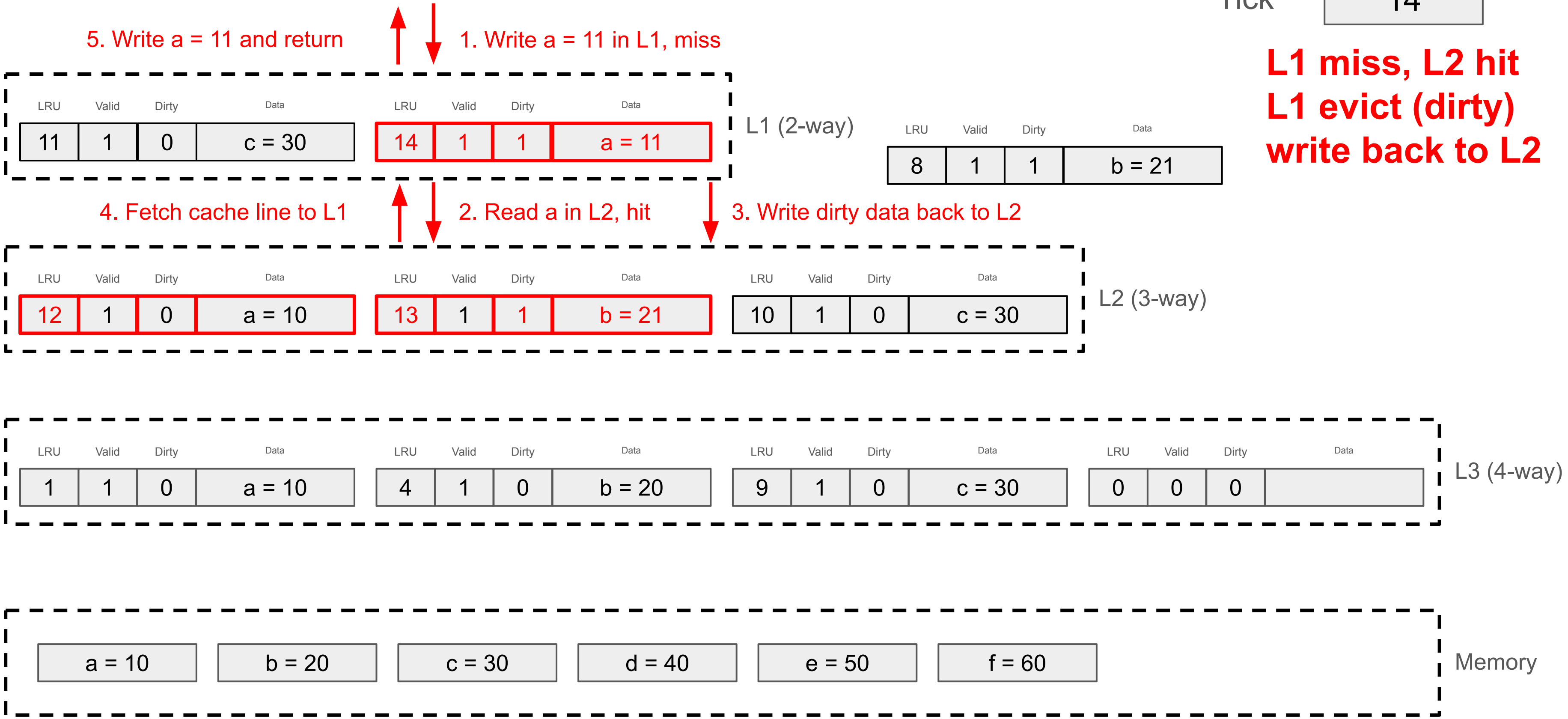
Cache line affected
LRU
Valid
Dirty
Data
7
1
0
a = 10
Tick
11
9. Return c = 30
1. Read c in L1, miss
7. Drop not dirty data
L1, L2, L3 miss
L1 evict (not dirty)
11
1
0
c = 30
8
1
1
b = 21
L1 (2-way)
8. Fetch cache line to L1
2. Read c in L2, miss
2
1
0
a = 10
5
1
0
b = 20
10
1
0
c = 30
L2 (3-way)
6. Fetch cache line to L2
3. Read c in L3, miss
1
1
0
a = 10
4
1
0
b = 20
9
1
0
c = 30
0
0
0
L3 (4-way)
5. Fetch cache line to L3
4. Read c in memory
a = 10
b = 20
c = 30
d = 40
e = 50
f = 60
Memory

Cache line affected

Write a

Tick 14

L1 miss, L2 hit
L1 evict (dirty)
write back to L2


5. Write a = 11 and return
1. Write a = 11 in L1, miss
4. Fetch cache line to L1
2. Read a in L2, hit
3. Write dirty data back to L2
L1 (2-way)
L2 (3-way)
L3 (4-way)
Memory

L1 (2-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
11	1	0	c = 30	14	1	1	a = 11

LRU	Valid	Dirty	Data
8	1	1	b = 21

L2 (3-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
12	1	0	a = 10	13	1	1	b = 21	10	1	0	c = 30

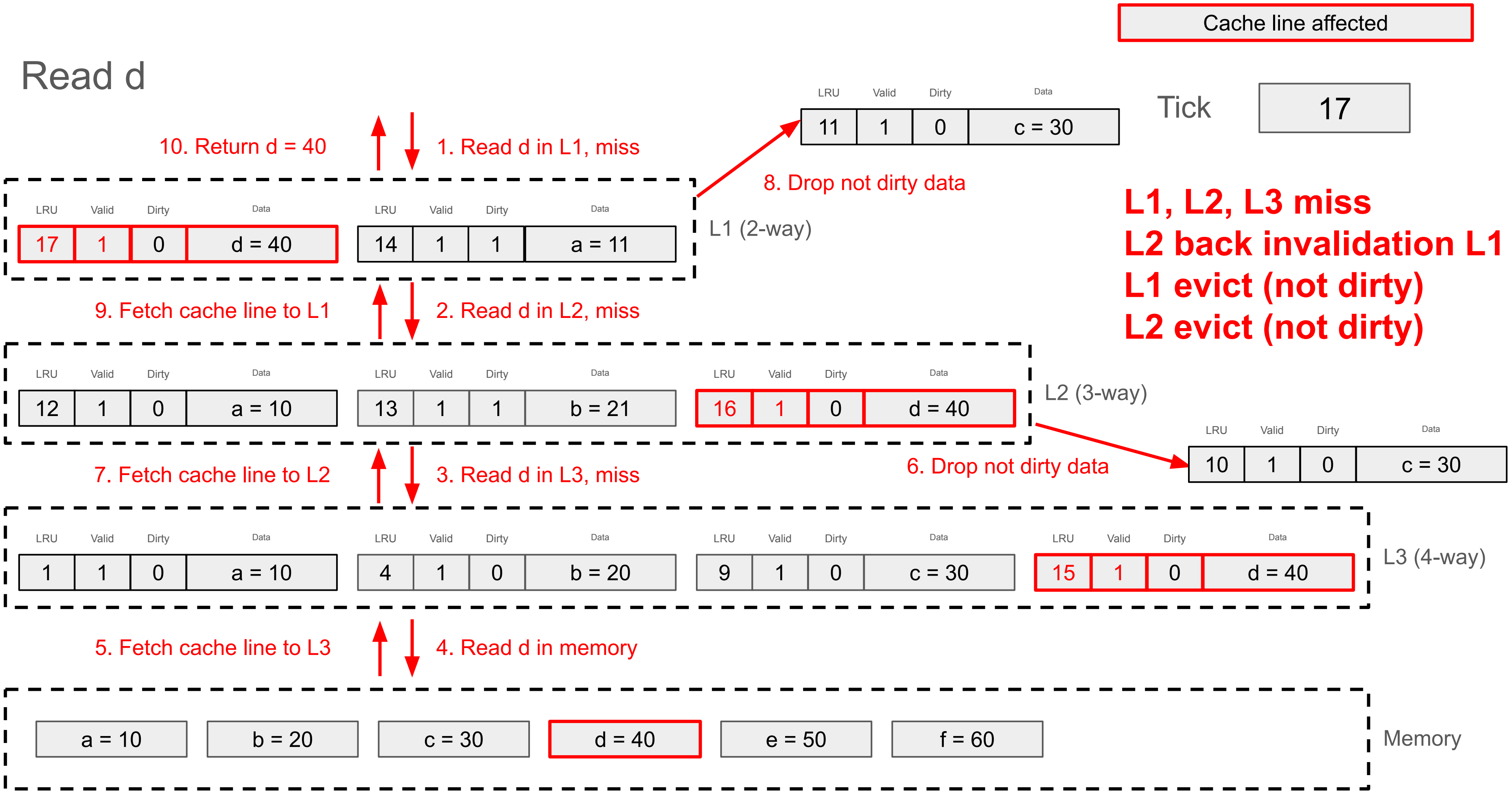
L3 (4-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
1	1	0	a = 10	4	1	0	b = 20	9	1	0	c = 30	0	0	0	

Memory

a = 10	b = 20	c = 30	d = 40	e = 50	f = 60

Read d



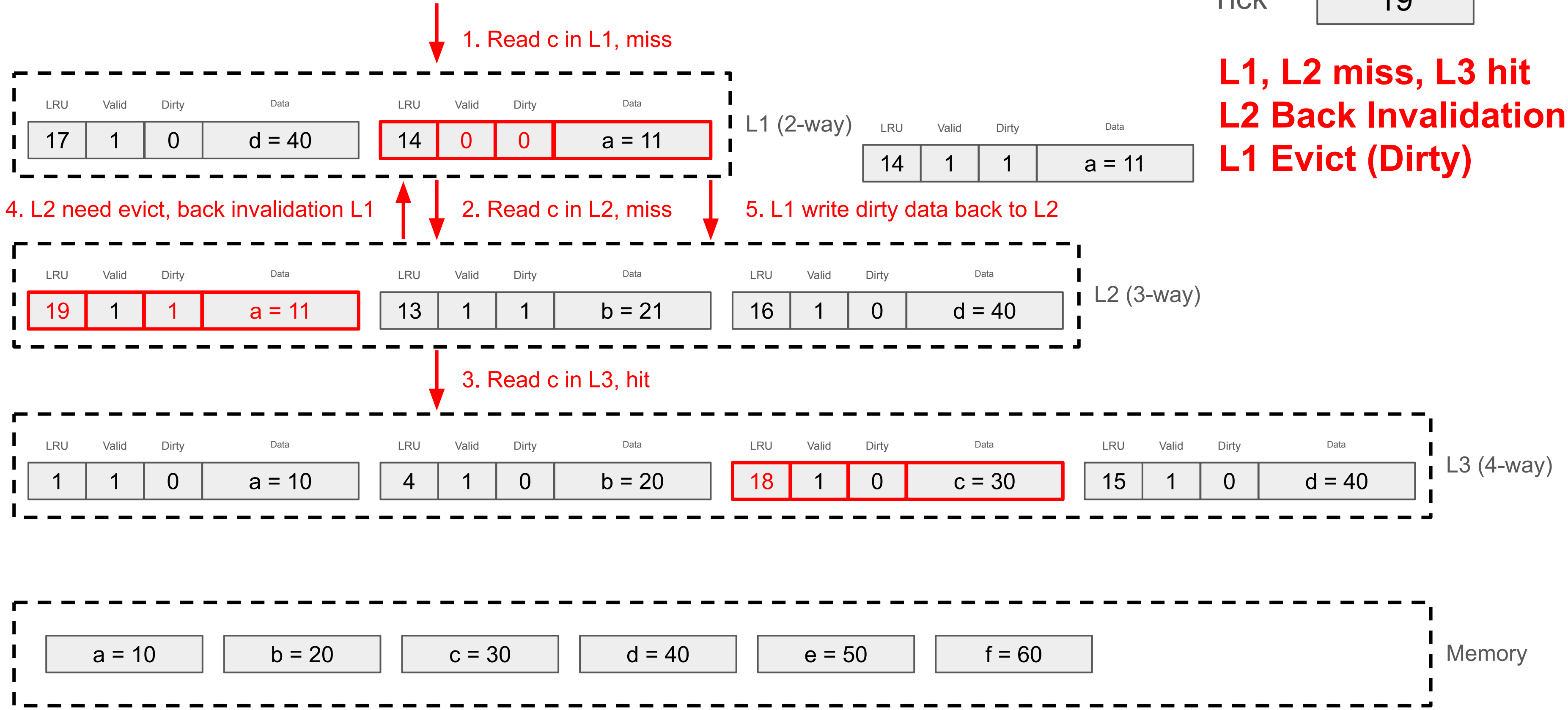
L1, L2, L3 miss
L2 back invalidation L1
L1 evict (not dirty)
L2 evict (not dirty)

Read c (cont'd)

Cache line affected

Tick 19

L1, L2 miss, L3 hit
L2 Back Invalidation
L1 Evict (Dirty)



L1 (2-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
17	1	0	d = 40	14	0	0	a = 11

LRU	Valid	Dirty	Data
14	1	1	a = 11

L2 (3-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
19	1	1	a = 11	13	1	1	b = 21	16	1	0	d = 40

L3 (4-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
1	1	0	a = 10	4	1	0	b = 20	18	1	0	c = 30	15	1	0	d = 40

Memory

a = 10	b = 20	c = 30	d = 40	e = 50	f = 60

Cache line affected

Read c (cont’d)

Tick 20

L1, L2 miss, L3 hit
L2 Back Invalidation
L1 Evict (Dirty)
L2 Evict (Dirty)

L1 (2-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
17	1	0	d = 40	14	0	0	a = 11

L2 (3-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
19	0	0	a = 11	13	1	1	b = 21	16	1	0	d = 40

LRU	Valid	Dirty	Data
19	1	1	a = 11

6. L1 write dirty data back to L2

L3 (4-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
20	1	1	a = 11	4	1	0	b = 20	18	1	0	c = 30	15	1	0	d = 40

Memory

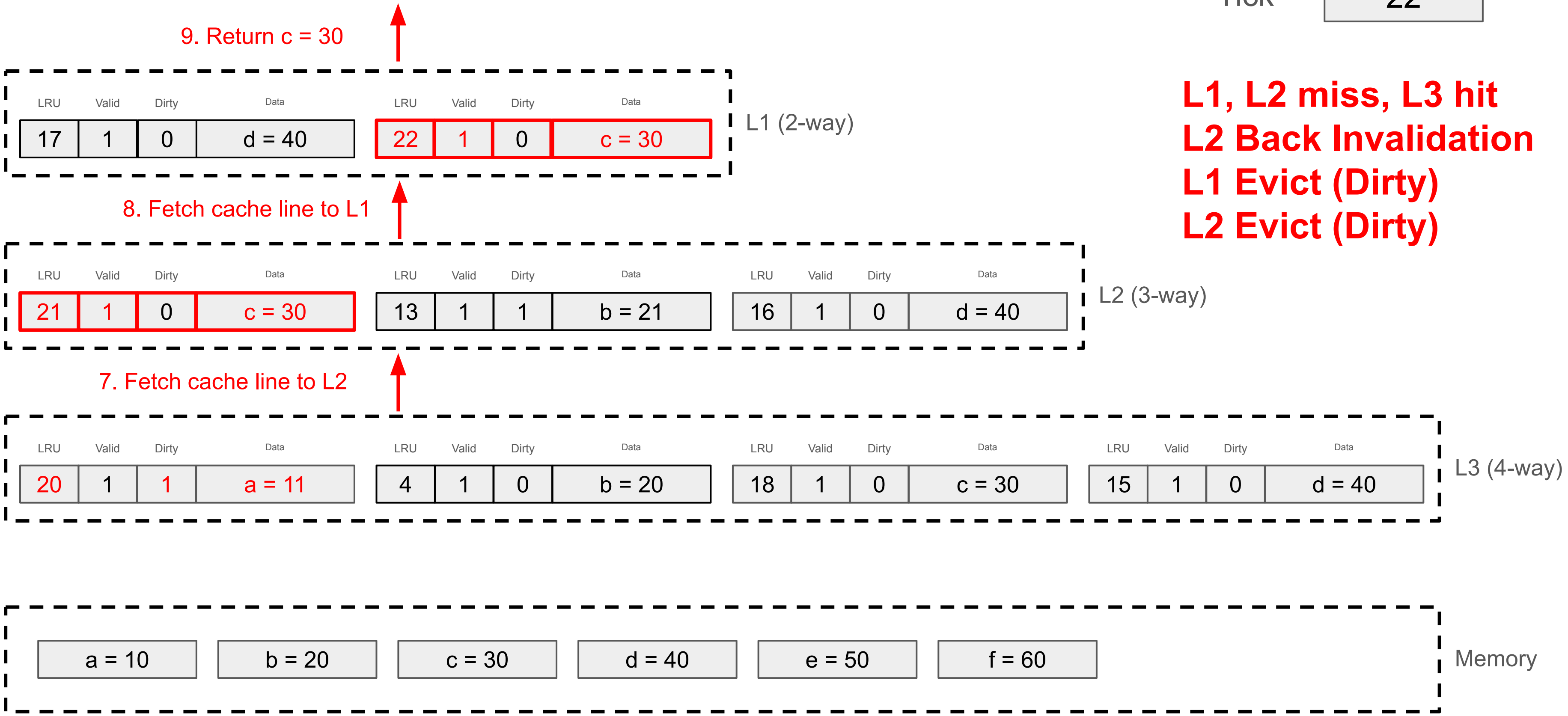
a = 10	b = 20	c = 30	d = 40	e = 50	f = 60

Read c

Cache line affected

Tick 22

L1, L2 miss, L3 hit
L2 Back Invalidation
L1 Evict (Dirty)
L2 Evict (Dirty)



L1 (2-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
17	1	0	d = 40	22	1	0	c = 30

L2 (3-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
21	1	0	c = 30	13	1	1	b = 21	16	1	0	d = 40

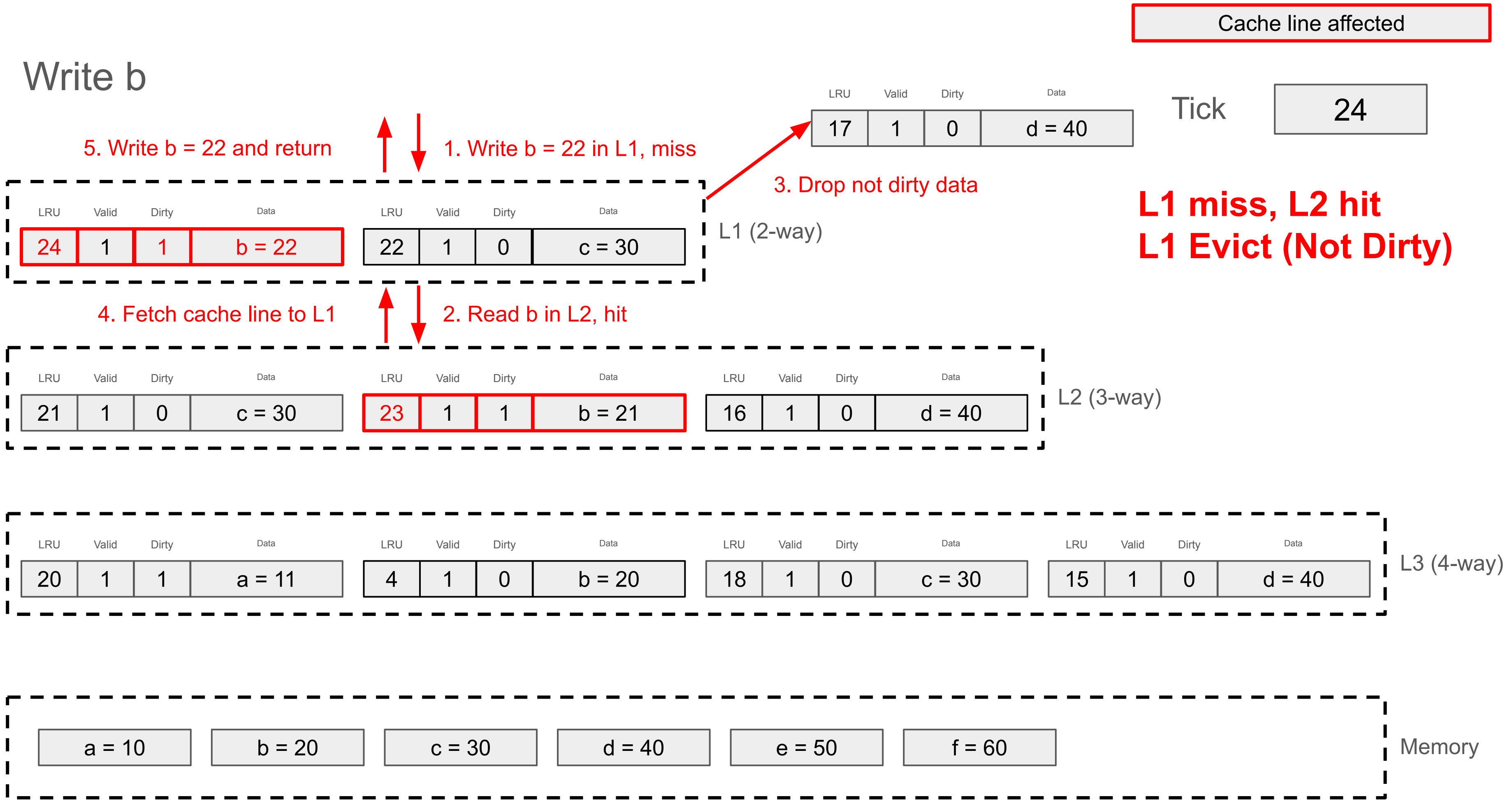
L3 (4-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
20	1	1	a = 11	4	1	0	b = 20	18	1	0	c = 30	15	1	0	d = 40

Memory

a = 10	b = 20	c = 30	d = 40	e = 50	f = 60

Write b



L1 miss, L2 hit
L1 Evict (Not Dirty)

Evicted line:

LRU	Valid	Dirty	Data
17	1	0	d = 40

L1 (2-way):

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
24	1	1	b = 22	22	1	0	c = 30

L2 (3-way):

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
21	1	0	c = 30	23	1	1	b = 21	16	1	0	d = 40

L3 (4-way):

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
20	1	1	a = 11	4	1	0	b = 20	18	1	0	c = 30	15	1	0	d = 40

Memory:

a = 10	b = 20	c = 30	d = 40	e = 50	f = 60

Cache line affected

Write c

Tick 25

L1 hit

3. Write c = 31 and return

1. Write c = 31 in L1, hit

L1 (2-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
24	1	1	b = 22	25	1	1	c = 31

L2 (3-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
21	1	0	c = 30	23	1	1	b = 21	16	1	0	d = 40

L3 (4-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
20	1	1	a = 11	4	1	0	b = 20	18	1	0	c = 30	15	1	0	d = 40

Memory

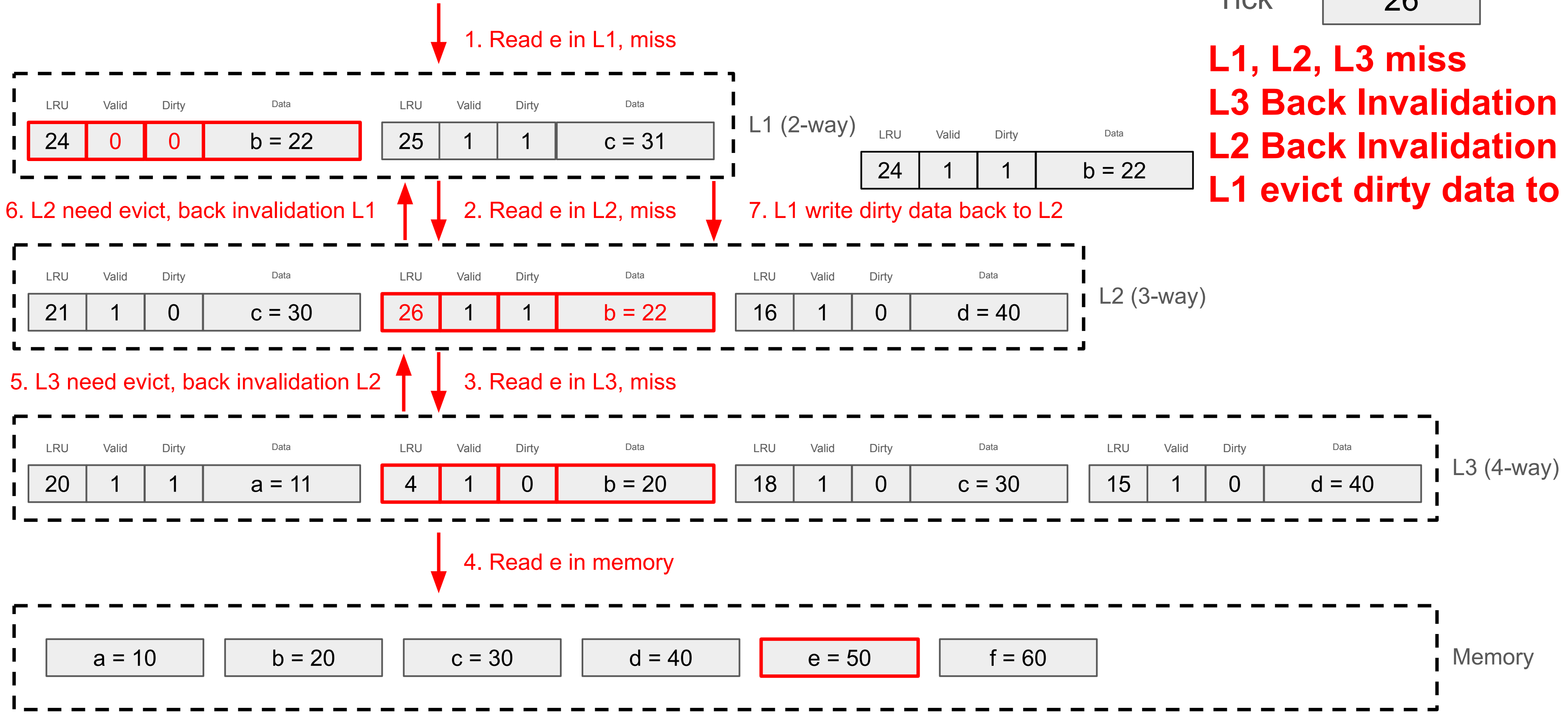
a = 10	b = 20	c = 30	d = 40	e = 50	f = 60

Cache line affected

Read e (cont'd)

Tick 26

L1, L2, L3 miss
L3 Back Invalidation L2
L2 Back Invalidation L1
L1 evict dirty data to L2



L1 (2-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
24	0	0	b = 22	25	1	1	c = 31

LRU	Valid	Dirty	Data
24	1	1	b = 22

L2 (3-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
21	1	0	c = 30	26	1	1	b = 22	16	1	0	d = 40

L3 (4-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
20	1	1	a = 11	4	1	0	b = 20	18	1	0	c = 30	15	1	0	d = 40

Memory

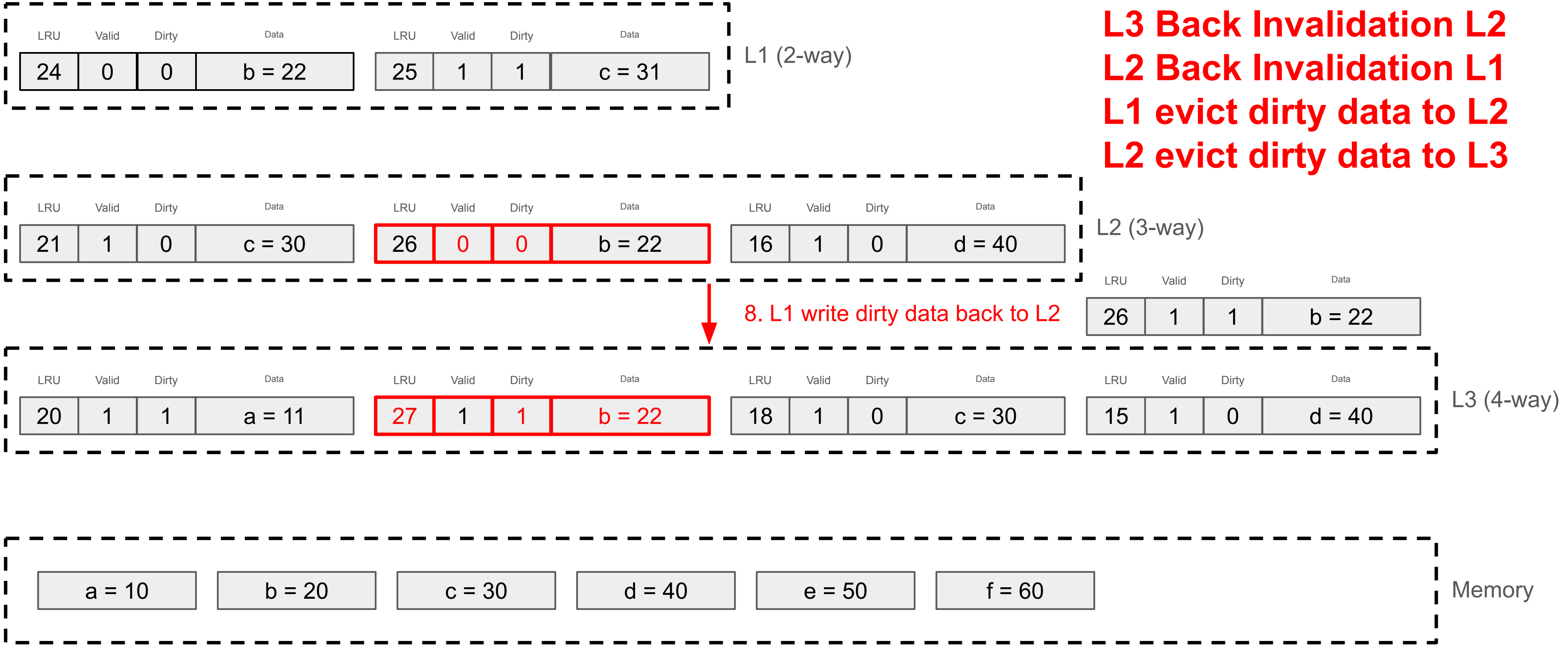
a = 10	b = 20	c = 30	d = 40	e = 50	f = 60

Cache line affected

Read e (cont'd)

Tick 27

L1, L2, L3 miss
L3 Back Invalidation L2
L2 Back Invalidation L1
L1 evict dirty data to L2
L2 evict dirty data to L3



L1 (2-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
24	0	0	b = 22	25	1	1	c = 31

L2 (3-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
21	1	0	c = 30	26	0	0	b = 22	16	1	0	d = 40

8. L1 write dirty data back to L2

LRU	Valid	Dirty	Data
26	1	1	b = 22

L3 (4-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
20	1	1	a = 11	27	1	1	b = 22	18	1	0	c = 30	15	1	0	d = 40

Memory

a = 10	b = 20	c = 30	d = 40	e = 50	f = 60

Cache line affected

Read e (cont'd)

Tick 27

L1, L2, L3 miss
L3 Back Invalidation L2
L2 Back Invalidation L1
L1 evict dirty data to L2
L2 evict dirty data to L3
L3 evict dirty data to Memory

L1 (2-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
24	0	0	b = 22	25	1	1	c = 31

L2 (3-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
21	1	0	c = 30	26	0	0	b = 22	16	1	0	d = 40

8. L2 write dirty data back to L3

LRU	Valid	Dirty	Data
26	1	1	b = 22

L3 (4-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
20	1	1	a = 11	27	0	0	b = 22	18	1	0	c = 30	15	1	0	d = 40

9. L3 write dirty data back to Memory

LRU	Valid	Dirty	Data
27	1	1	b = 22

Memory

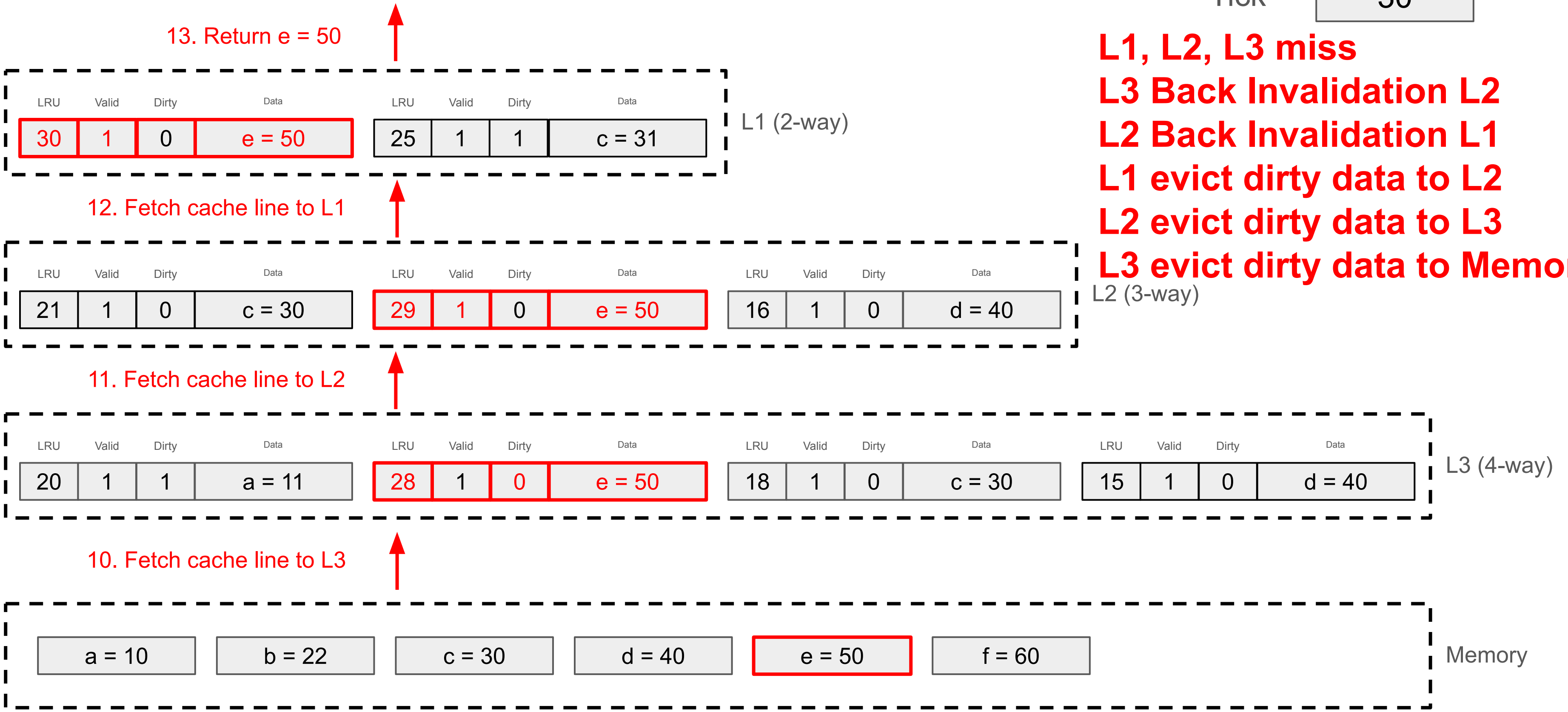
a = 10	b = 22	c = 30	d = 40	e = 50	f = 60

🟥 Cache line affected

Read e

Tick 30

L1, L2, L3 miss
L3 Back Invalidation L2
L2 Back Invalidation L1
L1 evict dirty data to L2
L2 evict dirty data to L3
L3 evict dirty data to Memory


13. Return e = 50
12. Fetch cache line to L1
11. Fetch cache line to L2
10. Fetch cache line to L3

L1 (2-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
30	1	0	e = 50	25	1	1	c = 31

L2 (3-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
21	1	0	c = 30	29	1	0	e = 50	16	1	0	d = 40

L3 (4-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
20	1	1	a = 11	28	1	0	e = 50	18	1	0	c = 30	15	1	0	d = 40

Memory

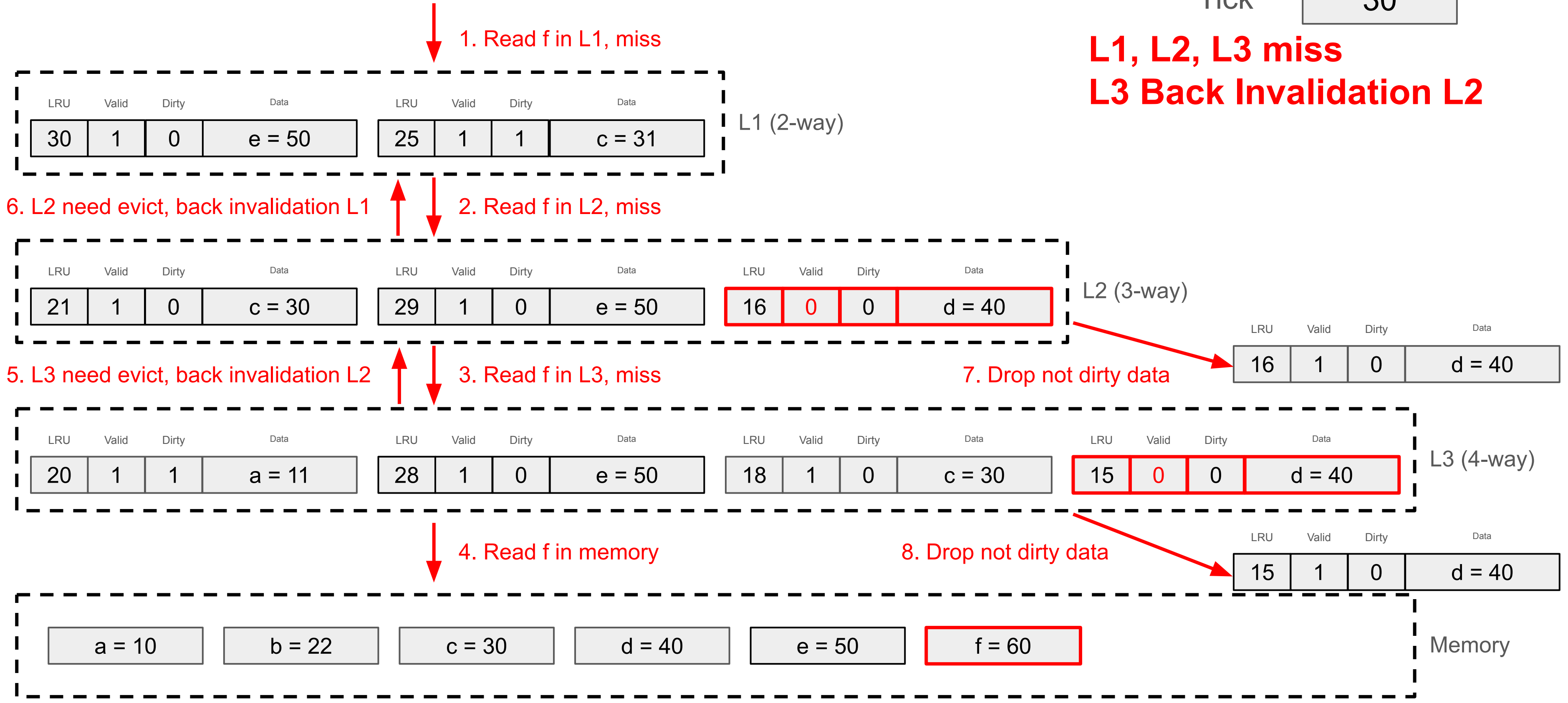
a = 10	b = 22	c = 30	d = 40	e = 50	f = 60

Read f (cont'd)

Cache line affected

Tick 30

L1, L2, L3 miss
L3 Back Invalidation L2



L1 (2-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
30	1	0	e = 50	25	1	1	c = 31

L2 (3-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
21	1	0	c = 30	29	1	0	e = 50	16	0	0	d = 40

7. Drop not dirty data

LRU	Valid	Dirty	Data
16	1	0	d = 40

L3 (4-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
20	1	1	a = 11	28	1	0	e = 50	18	1	0	c = 30	15	0	0	d = 40

8. Drop not dirty data

LRU	Valid	Dirty	Data
15	1	0	d = 40

Memory

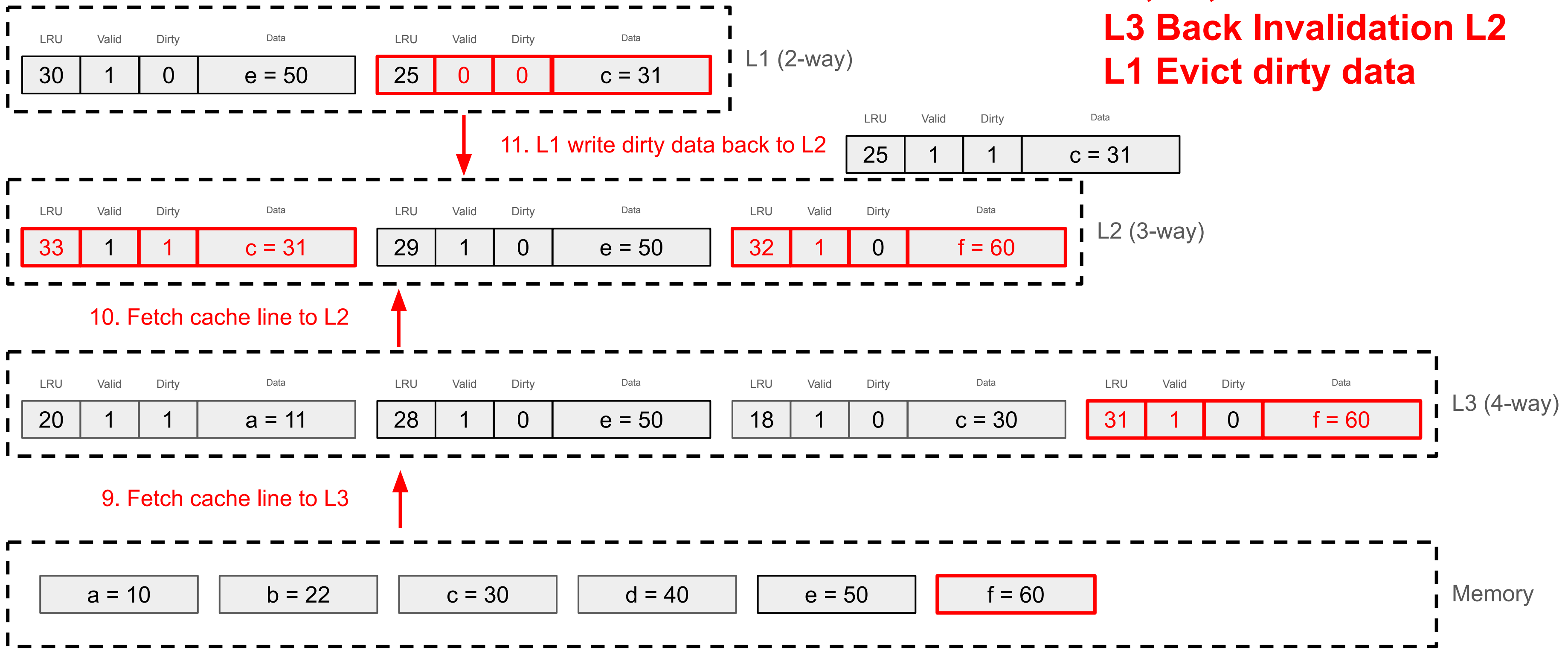
a = 10	b = 22	c = 30	d = 40	e = 50	f = 60

Read f (cont'd)

Cache line affected

Tick 30

L1, L2, L3 miss
L3 Back Invalidation L2
L1 Evict dirty data

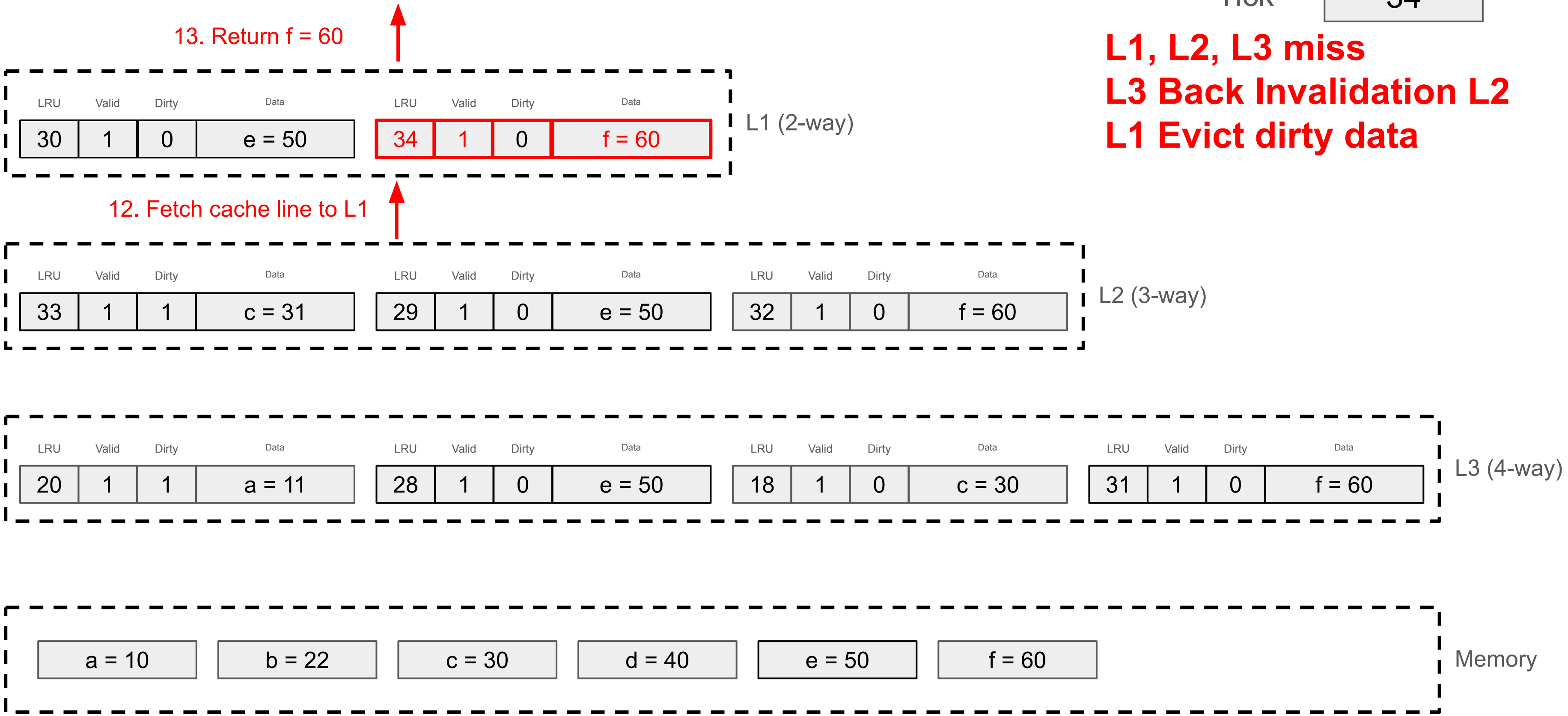


Read f

Cache line affected

Tick 34

L1, L2, L3 miss
L3 Back Invalidation L2
L1 Evict dirty data



L1 (2-way)

LRU	Valid	Dirty	Data
30	1	0	e = 50
34	1	0	f = 60

L2 (3-way)

LRU	Valid	Dirty	Data
33	1	1	c = 31
29	1	0	e = 50
32	1	0	f = 60

L3 (4-way)

LRU	Valid	Dirty	Data
20	1	1	a = 11
28	1	0	e = 50
18	1	0	c = 30
31	1	0	f = 60

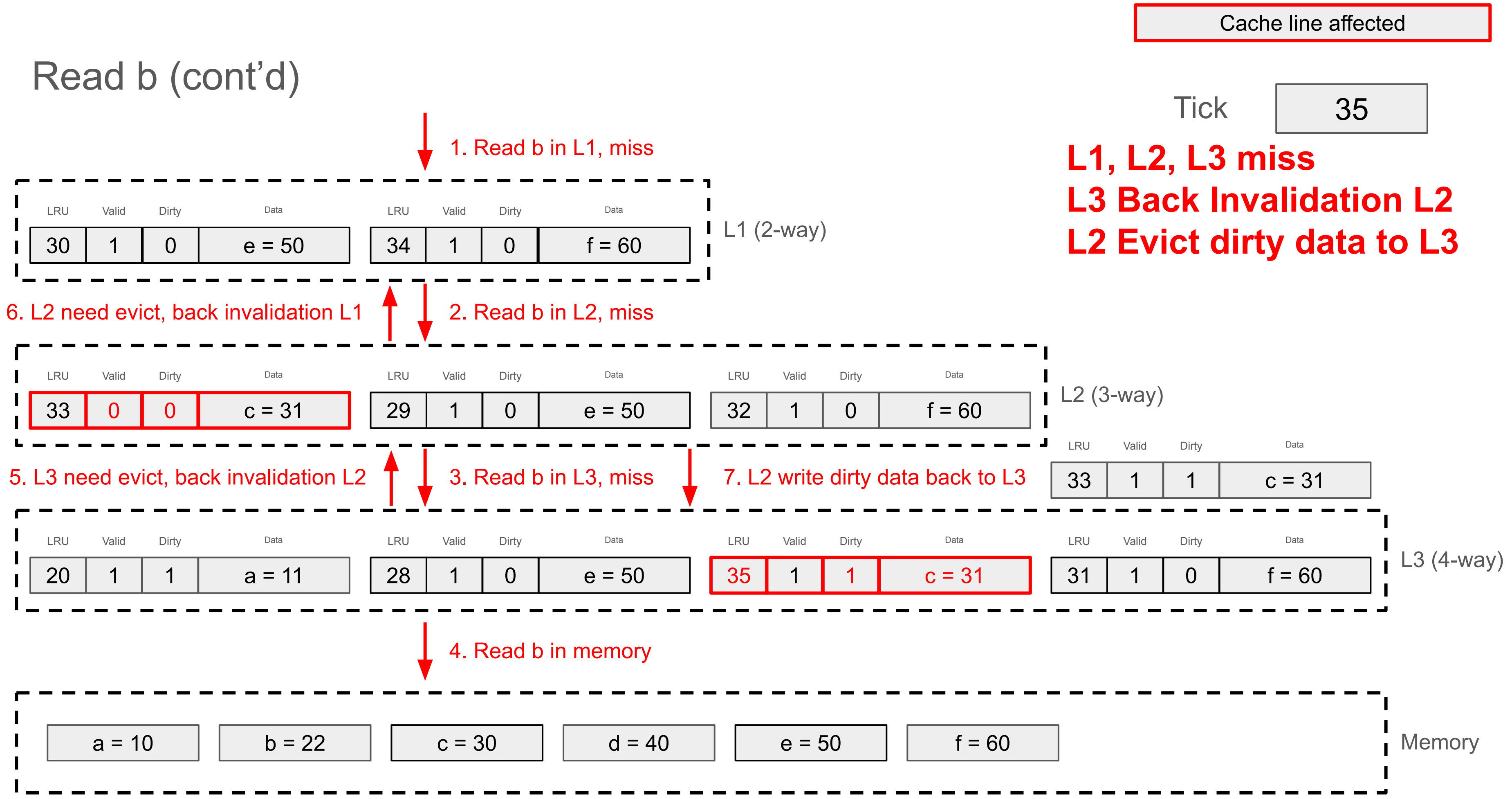
Memory

a = 10	b = 22	c = 30	d = 40	e = 50	f = 60

Read b (cont'd)

Tick 35

L1, L2, L3 miss
L3 Back Invalidation L2
L2 Evict dirty data to L3



Cache line affected

Read b (cont'd)

Tick 34

L1, L2, L3 miss
L3 Back Invalidation L2
L2 Evict dirty data to L3
L3 Evict dirty data to memory

L1 (2-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
30	1	0	e = 50	34	1	0	f = 60

L2 (3-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
33	0	0	c = 31	29	1	0	e = 50	32	1	0	f = 60

L3 (4-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
20	1	1	a = 11	28	1	0	e = 50	35	0	0	c = 31	31	1	0	f = 60

8. L3 write dirty data back to Memory

LRU	Valid	Dirty	Data
34	1	1	c = 31

Memory

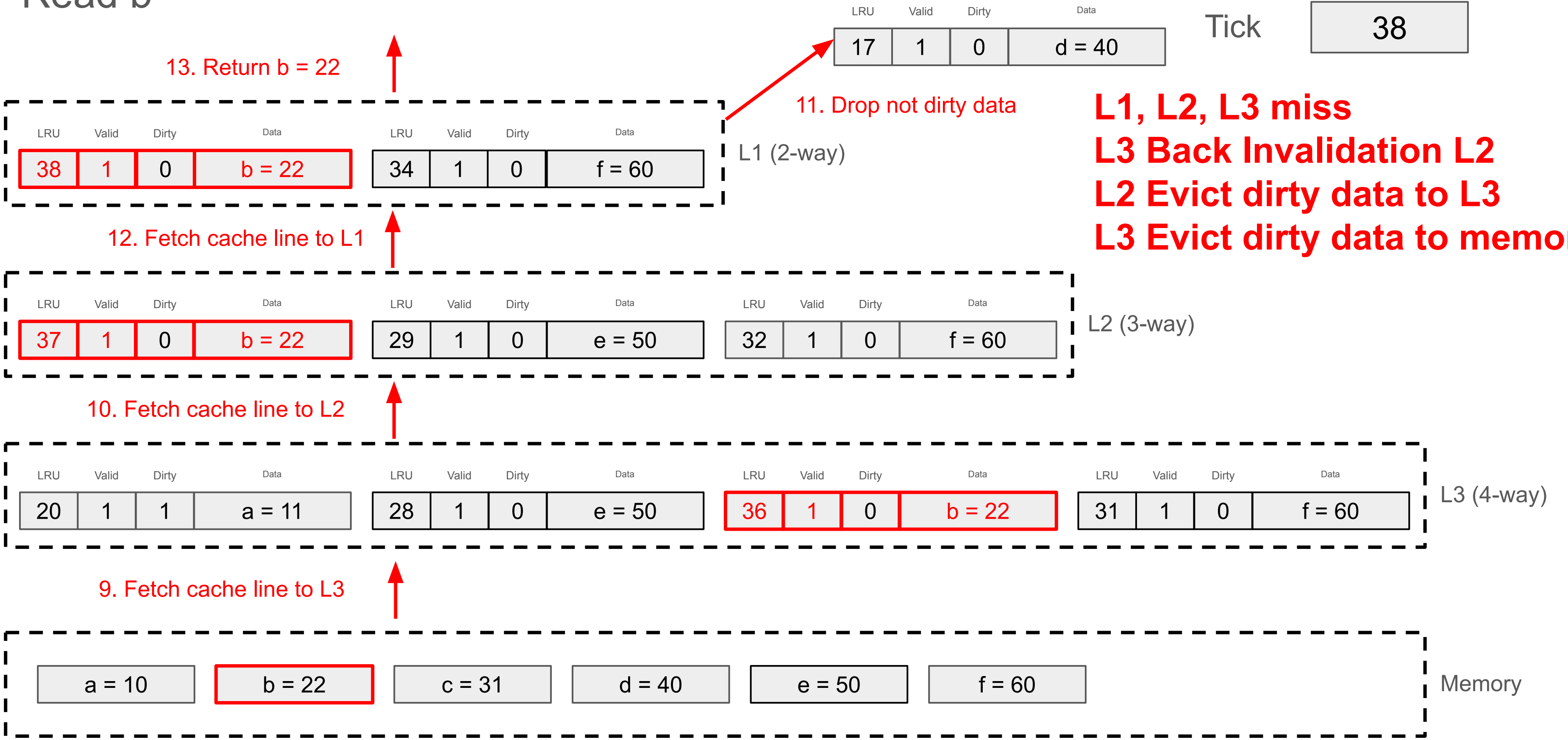
a = 10	b = 22	c = 31	d = 40	e = 50	f = 60

Cache line affected

Read b

Tick 38

L1, L2, L3 miss
L3 Back Invalidation L2
L2 Evict dirty data to L3
L3 Evict dirty data to memory

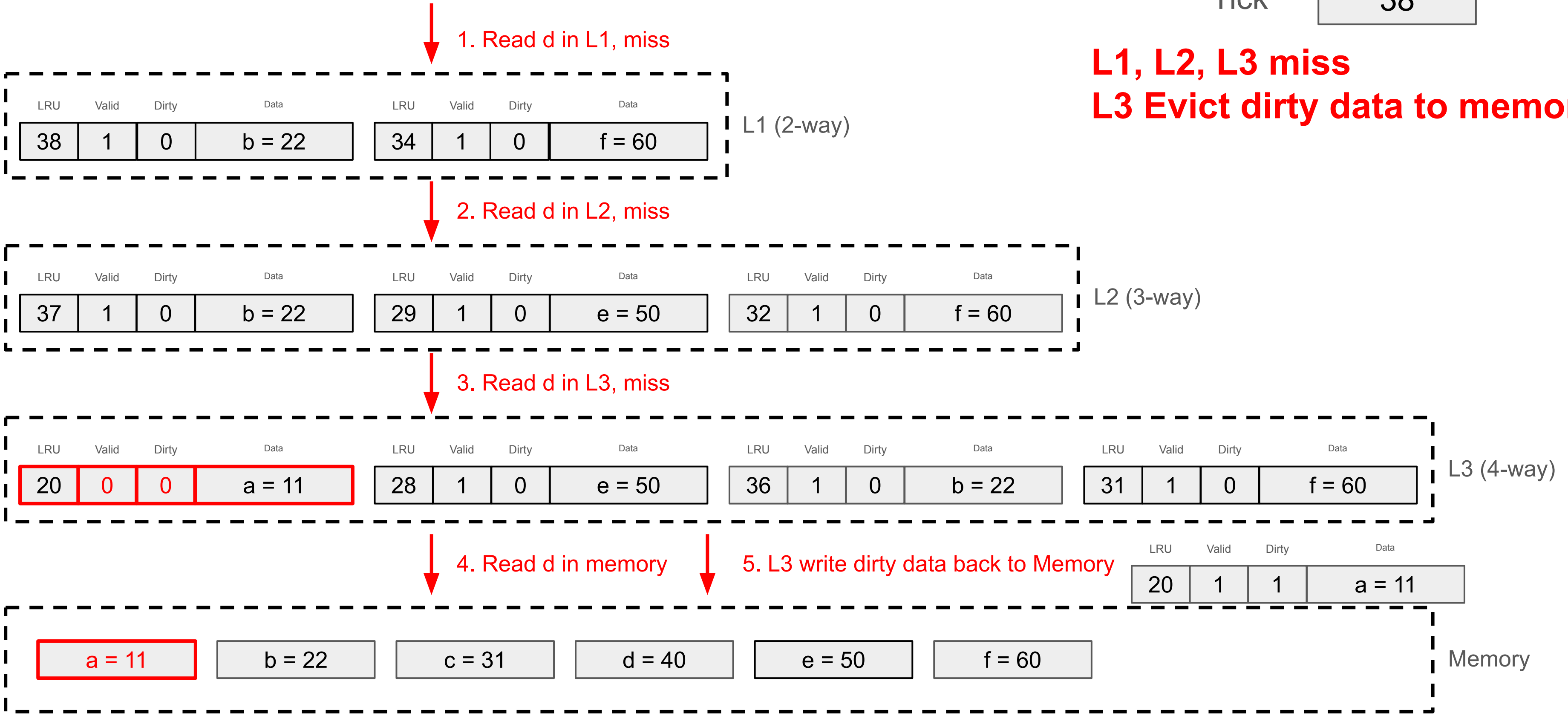


Cache line affected

Read d (cont'd)

Tick 38

L1, L2, L3 miss
L3 Evict dirty data to memory



1. Read d in L1, miss

L1 (2-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
38	1	0	b = 22	34	1	0	f = 60

2. Read d in L2, miss

L2 (3-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
37	1	0	b = 22	29	1	0	e = 50	32	1	0	f = 60

3. Read d in L3, miss

L3 (4-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
20	0	0	a = 11	28	1	0	e = 50	36	1	0	b = 22	31	1	0	f = 60

4. Read d in memory

5. L3 write dirty data back to Memory

LRU	Valid	Dirty	Data
20	1	1	a = 11

Memory

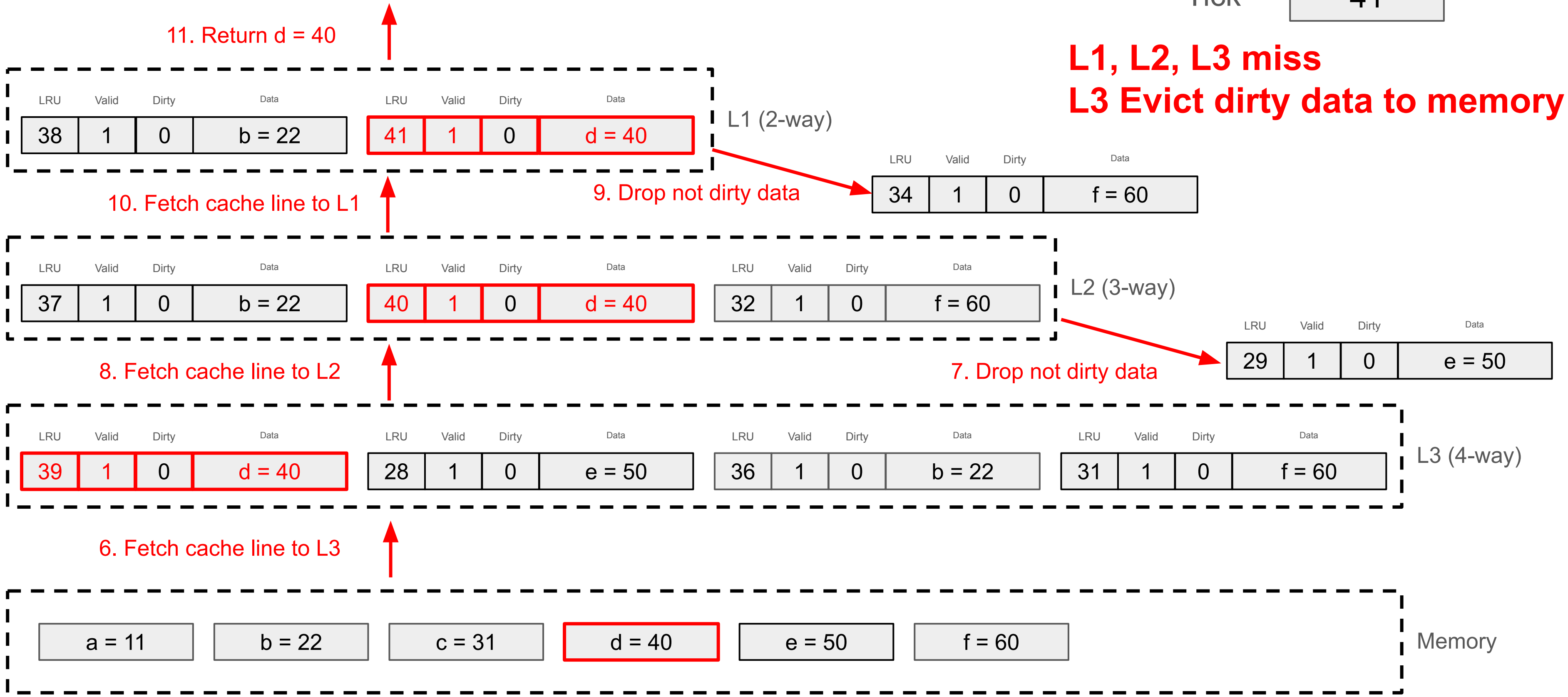
a = 11	b = 22	c = 31	d = 40	e = 50	f = 60

Cache line affected

Read d

Tick 41

L1, L2, L3 miss
L3 Evict dirty data to memory



L1 (2-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
38	1	0	b = 22	41	1	0	d = 40

9. Drop not dirty data

LRU	Valid	Dirty	Data
34	1	0	f = 60

L2 (3-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
37	1	0	b = 22	40	1	0	d = 40	32	1	0	f = 60

7. Drop not dirty data

LRU	Valid	Dirty	Data
29	1	0	e = 50

L3 (4-way)

LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data	LRU	Valid	Dirty	Data
39	1	0	d = 40	28	1	0	e = 50	36	1	0	b = 22	31	1	0	f = 60

Memory

a = 11	b = 22	c = 31	d = 40	e = 50	f = 60